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10/799,039	03/11/2004	Charles C. Lee	3030P	6726

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,039	LEE ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-18,21-32,35-46 and 49-56* is/are rejected.

7)☒ Claim(s) *5,6,19,20,33,34,47 and 48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-56 are presented for examination.

Information Disclosure Statement

2. The IDS filed on 09/20/2004 has been received and carefully considered.

3. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This request is not intended to interfere with or go beyond that required under 37 C.F.R. 1 .56 or 1 .105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1 .97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request

and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1 .97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs, etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. "utilizing an internal buffer within the flash memory device to store valid data during the search before the valid data is relocated" aspect of the invention should be mentioned in the title so that the title is more descriptive.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the processor within the flash memory controller" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2, 16, 30, 39-42, 44 and 53-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The phrase "the flash memory device comprises a plurality of flash memory devices" is unclear in claims 2, 16, 30 and 44. It seems to be a *recursive definition.*

8. Claims 39-42 and 53-56 recite the limitation "the flash memory controller" in line 1. There is insufficient antecedent basis for this limitation in these claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 12-13, 15 and 26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Cruz (USPN: 2005/0102444).

As per claim 1, Cruz teaches a flash memory controller (i.e. 12 in Fig. 1) comprising: a processor (i.e. 24 in Fig. 1) for performing at least one operation (i.e. requesting data transfers to and from the SDRAM 52 in Fig. 1); and arbitration logic (i.e. 99 in Fig. 1) coupled to the processor, wherein data from the arbitration logic allows the processor to perform the at least one operation for a flash memory device (i.e. 48 in Fig. 1) (e.g. see paragraph [0021] and Fig. 1).

As per claim 12, Cruz teaches the claimed invention as described above and furthermore, Cruz teaches that the flash memory controller (i.e. 12 in Fig. 1) provides dual channel processing (i.e. processing via buses 46 and 50 in Fig. 1) (e.g. see Fig. 1).

As per claim 13, Cruz teaches the claimed invention as described above and furthermore, Cruz teaches that the flash memory controller (i.e. 12 in Fig. 1) can perform multiple banks interleave (i.e. accessing multiple banks 48 and 52 via buses 46 and 50 in Fig. 1) (e.g. see Fig. 1).

As per claim 15, Cruz teaches a flash memory system comprising: a first processor (i.e. 24 in Fig. 1); a device interface (i.e. 28 in Fig. 1) coupled to the processor; and a flash memory controller (i.e. 36 in Fig. 1) coupled to the device interface, the flash memory controller comprising: a second processor (i.e. 54 in Fig. 1) for executing at least one operation; and arbitration logic (i.e. 96 in Fig. 1) coupled to the processor, wherein data from the arbitration logic allows the processor to perform the at least one operation for a flash memory device (i.e. 48 in Fig. 1) (e.g. see paragraph [0021] and Fig. 1).

As per claims 26-27, see arguments with respect to the rejection of claims 12-13, respectively. Claims 26 and 27 are also rejected based on the same rationale as the rejection of claims 12-13, respectively.

10. Claims 29 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (USPN: 5,907,856) hereinafter, Estakhri.

As per claim 29, Estakhri teaches a method for managing flash memory in a flash memory system, the method comprising: (a) initiating at least one operation (i.e. by sending the write instruction, 200 in Fig. 9); (b) conducting a search for a destination block within a flash memory device (i.e. 508 in Fig. 10); and (c) relocating valid data (i.e. the new data/information) within the flash memory device from a source block to the destination block, wherein the at least one operation is performed for the flash memory device, i.e. first making sure that the information is first being erased before writing the new data/information, and then writing the new data identified by the PBA (e.g. see Col. 10, lines 15-21 and Figs. 9-10).

As per claim 43, see arguments with respect to the rejection of claim 29. Claim 43 is also rejected based on the same rationale as the rejection of claim 29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7-10 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cruz in view of the Applicant's Admitted Prior Art, hereinafter, AAPA.

As per claims 7 and 8, Cruz teaches the claimed invention as described above, but failed to teach that the operation comprises at least one block management operation; and the at least one block management operation comprises one of handling bad blocks, recycling obsolete blocks, and wear leveling. AAPA, however, discloses that the operation comprises at least one block management operation (i.e. the erase operation), i.e. recycling/erasing obsolete blocks (e.g. see lines 5-10 on page 9 of the current application). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement AAPA's teachings in the method taught by Cruz by performing the block management operation (i.e. the erase operation), i.e. recycling/erasing obsolete blocks operation, so they become available for future write operations, i.e. the number of available memory blocks in the flash memory increases and therefore, the overall performance of the flash memory controller improves.

As per claims 9 and 10, Cruz teaches the claimed invention as described above and furthermore, Cruz teaches that the flash memory controller (i.e. 12 in Fig. 1) is bidirectionally coupled and applied the NAND flash memory (i.e. 48 in Fig. 1) via the flash bus (i.e. 46 in Fig. 1) and the NAND flash controller (i.e. 40 in Fig. 1) (e.g. see paragraph [0017] and Fig. 1). However, Cruz does not disclose different types of flash memories. AAPA, however, discloses different types of flash memories, for example,

Universal Serial Bus (USB) Drive, Secure Digital card (SD), MultiMediaCard (MMC), Memory Stick (MS), Compact Flash (CF) Card, ExpressCard, Flash Memory Hard Drive, etc., which are used as storage media in the mass-storage systems because unlike the magnetic storage devices, the flash memory has lower power dissipation and smaller physical sizes; and provides higher storage capacity and faster access speeds (e.g. see lines 7-15 on page 1). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to use different types of flash memories as taught by AAPA in the flash controller taught by Cruz. In doing so, different types of flash memories can be use in the mobile systems because of its compatibility (e.g. see lines 7-15 on page 1 of the current application).

As per claims 21-24, see arguments with respect to the rejection of claims 7-10, respectively. Claims 21-24 are also rejected based on the same rationale as the rejection of claims 7-10, respectively.

12. Claims 2-4, 11, 14, 16-18, 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cruz in view of Kuo et al. (USPN: 6,275,894) hereinafter, Kuo.

As per claims 2 and 3, Cruz teaches the claimed invention as described above. However, Cruz does not teach that the flash memory device comprises a plurality of flash memory devices having different capacities. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture comprising a plurality of flash memory devices (i.e. the upper and the lower memory banks) having different capacities (i.e. different memory bank sizes) (e.g. see Col. 3, lines 4-16). Accordingly, it

would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the flash memory controller of Cruz so the flash memory device with a flexible bank partition architecture is realized without the costs and efforts associated with designing different circuits; and different sets of masks for meeting the requirements of different memory bank sizes to produce different conventional simultaneous operation flash memory devices with fixed upper and lower bank partitions can be prepared.

As per claim 4, the combination of Cruz and Kuo teaches the claimed invention as described and furthermore, Kuo teaches that the at least one operation can be performed simultaneously on different flash memory devices of the flash memory system (e.g. see Col. 3, lines 4-16).

As per claim 11, Cruz teaches the claimed invention as described above. However, Cruz does not teach that the flash memory controller provides multiple-block data access. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture, in which, different sets of masks for meeting the requirements of different memory bank sizes to produce different conventional simultaneous operation flash memory devices with fixed upper and lower bank partitions can be prepared (e.g. see Col. 3, lines 4-16). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the flash memory controller of Cruz so the memory transactions can be executed twice as fast. Therefore, the overall performance of the flash memory controller increases.

As per claim 14, Cruz teaches the claimed invention as described above and furthermore, Cruz teaches that the flash memory controller (i.e. 12 in Fig. 1) can perform functions of multiple block access (i.e. accessing multiple banks 48 and 52 via buses 46 and 50 in Fig. 1), multiple bank interleaving (i.e. accessing multiple banks 48 and 52 via buses 46 and 50 in Fig. 1) and multiple channel operations (i.e. via buses 46 and 50 in Fig. 1) (e.g. see Fig. 1). However, Cruz failed to teach that the flash memory controller could perform these functions in a memory cycle. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture in which different conventional simultaneous operations (i.e. within a memory cycle) can be performed on the upper and lower bank partitions of the flash memory (e.g. see Col. 3, lines 4-16). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the flash memory controller of Cruz so the memory transactions can be executed twice as fast. Therefore, the overall performance of the flash memory controller increases.

As per claims 16-18, 25 and 28, see arguments with respect to the rejection of claims 2-4, 11 and 14, respectively. Claims 16-18, 25 and 28 are also rejected based on the same rationale as the rejection of claims 2-4, 11 and 14, respectively.

13. Claims 30-32, 39, 44-46 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of Kuo.

As per claims 30 and 31, Cruz teaches the claimed invention as described above. However, Estakhri does not teach that the flash memory device comprises a

plurality of flash memory devices having different capacities. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture comprising a plurality of flash memory devices (i.e. the upper and the lower memory banks) having different capacities (i.e. different memory bank sizes) (e.g. see Col. 3, lines 4-16). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the method of Estakhri so the flash memory device with a flexible bank partition architecture is realized without the costs and efforts associated with designing different circuits; and different sets of masks for meeting the requirements of different memory bank sizes to produce different conventional simultaneous operation flash memory devices with fixed upper and lower bank partitions can be prepared.

As per claim 32, the combination of Cruz and Estakhri teaches the claimed invention as described and furthermore, Kuo teaches that the at least one operation can be performed simultaneously on different flash memory devices of the flash memory system (e.g. see Col. 3, lines 4-16).

As per claim 39, Estakhri teaches the claimed invention as described above. However, Estakhri does not teach that the flash memory controller provides multiple-block data access. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture, in which, different sets of masks for meeting the requirements of different memory bank sizes to produce different conventional simultaneous operation flash memory devices with fixed upper and lower bank partitions can be prepared (e.g. see Col. 3, lines 4-16). Accordingly, it would have been obvious

to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the flash memory controller of Estakhri so the memory transactions can be executed twice as fast. Therefore, the overall performance of the flash memory controller increases.

As per claims 44-46 and 53, see arguments with respect to the rejection of claims 30-32 and 39, respectively. Claims 44-46 and 53 are also rejected based on the same rationale as the rejection of claims 30-32 and 39, respectively.

14. Claims 40-42 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of Cruz, further in view of Kuo.

As per claims 40-42 and 54-56, Estakhri teaches the claimed invention as described above and furthermore, Estakhri teaches that the flash memory system comprising a flash memory controller (i.e. 532 in Fig. 10). However, Estakhri failed to teach that the flash memory controller can perform functions of multiple block data access, multiple bank interleaving and multiple channel operations in a memory access cycle. Cruz, on the other hand, teaches the flash memory controller (i.e. 12 in Fig. 1) that can perform functions of multiple block access (i.e. accessing multiple banks 48 and 52 via buses 46 and 50 in Fig. 1), multiple bank interleaving (i.e. accessing multiple banks 48 and 52 via buses 46 and 50 in Fig. 1) and multiple channel operations (i.e. via buses 46 and 50 in Fig. 1) (e.g. see Fig. 1). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to

implement Cruz's teachings in the flash memory controller of Estakhri so the memory transactions can be performed faster thru the multiple channels.

However, both Estakhri and Cruz failed to teach that the flash memory controller could perform these functions in a memory cycle. Kuo, on the other hand, teaches the flash memory device with a flexible bank partition architecture in which different conventional simultaneous operations (i.e. within a memory cycle) can be performed on the upper and lower bank partitions of the flash memory (e.g. see Col. 3, lines 4-16). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement Kuo's teachings in the flash memory system taught by the combination of Estakhri and Cruz so the memory transactions can be executed twice as fast. Therefore, the overall performance of the flash memory controller increases.

15. Claims 35-38 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri in view of AAPA.

As per claims 35 and 36, Estakhri teaches the claimed invention as described above, but failed to teach that the operation comprises at least one block management operation; and the at least one block management operation comprises one of handling bad blocks, recycling obsolete blocks, and wear leveling. AAPA, however, discloses that the operation comprises at least one block management operation (i.e. the erase operation), i.e. recycling/erasing obsolete blocks (e.g. see lines 5-10 on page 9 of the current application). Accordingly, it would have been obvious to one ordinary skilled in

the art at the time of the current invention was made to implement AAPA's teachings in the method taught by Estakhri by performing the block management operation (i.e. the erase operation), i.e. recycling/erasing obsolete blocks operation, so they become available for future write operations, i.e. the number of available memory blocks in the flash memory increases and therefore, the overall performance of the flash memory controller improves.

As per claims 37 and 38, Estakhri teaches the claimed invention as described above and furthermore, Estakhri teaches that the flash memory controller (i.e. 532 in Fig. 10) is coupled and applied the flash memory (i.e. 508 in Fig. 10) via the bus (i.e. 538 in Fig. 10) (e.g. see Fig. 10). However, Estakhri does not disclose different types of flash memories. AAPA, however, discloses different types of flash memories, for example, Universal Serial Bus (USB) Drive, Secure Digital card (SD), MultiMediaCard (MMC), Memory Stick (MS), Compact Flash (CF) Card, ExpressCard, Flash Memory Hard Drive, etc., which are used as storage media in the mass-storage systems because unlike the magnetic storage devices, the flash memory has lower power dissipation and smaller physical sizes; and provides higher storage capacity and faster access speeds (e.g. see lines 7-15 on page 1). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to use different types of flash memories as taught by AAPA in the flash controller taught by Estakhri. In doing so, different types of flash memories can be use in the mobile systems because of its compatibility (e.g. see lines 7-15 on page 1 of the current application).

As per claims 49-52, see arguments with respect to the rejection of claims 35-38, respectively. Claims 49-52 are also rejected based on the same rationale as the rejection of claims 35-38, respectively.

Allowable Subject Matter

16. Claims 5-6, 19-20, 33-34, 47 and 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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